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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,475	08/30/2001	Cliff Zitlaw	400.126US01	9305

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LEFFERT JAY & POLGLAZE, P.A.
P.O. BOX 581009
MINNEAPOLIS, MN 55458-1009

EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,475	ZITLAW, CLIFF	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 16-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 6, 16, 19 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Each of the above claims recites the limitation "dedicated bus." The original disclosure does not support this limitation. The closest support for this limitation can be found on page 2, paragraph 7, where the specification discloses a "flash memory device coupled to ... communicate with the synchronous memory device via a **direct bus**." The specification is silent as to whether this direct bus is dedicated or not.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 3 – 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Dye (US Patent No. 6,145,069).

With respect to claim 1, 3 and 5 Dye disclose a processing system comprising:

a processor that is adapted to write compressed data (figure 5, 400, col. 10, lines 3 – 8, col. 12, lines 10 – 14);

a volatile memory device coupled to communicate with the processor (160);

a non-volatile memory device (device consisting of circuits left of the data buffer 160 including 280 and 100) coupled to receive compressed data from the processor, the non-volatile memory device further connected to transfer data to the volatile memory device over a dedicated bus without intervention by another device (connection between 280, which is a part of the non-volatile device, and 160 is direct without any other intervening device); and

a decompression circuit (280) provided in the non-volatile memory device to decompress the data being transferred to the volatile memory device.

5. With respect to claim 4, the processor is coupled to store compressed data in the volatile memory device (col. 12, lines 10 – 14).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 5 – 7, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dye in view of Harari *et al.* (US Patent No. 6,266,724, hereinafter "Harari") and further in view of Fallon (US Patent Application Publication No. 2002/069354).

8. With respect to claims 5, 6 and 9, Dye discloses a processing system (figure 5) comprising:

a processor that is adapted to write compressed data (figure 5, 400, col. 10, lines 3 – 8, col. 12, lines 10 – 14) ;

a memory device (160) coupled to communicate with the processor via a bus;

a flash memory (device consisting of circuits left of the data buffer 160 including 280 and 100) device coupled to receive the compressed data from the processor via a bus and communicate with the memory device, wherein the flash memory device transfers data to the memory device over a dedicated bus without intervention by another device (see rejection of claim 1 above); and

a decompression circuit (280) provided in the flash memory device to decompress the data while transferring to the memory device.

However, Dye does not specifically disclose that the flash memory device is coupled to the processor via a serial bus. On the other hand, Harari discloses a flash memory device with a decompression circuit that is coupled to a processor via a serial bus (col. 7, lines 34 – 37).

It would have been obvious to one of ordinary skill in the art, having the teachings of Dye and Harari before him at the time the invention was made, to use the removable memory card that is couple via a serial bus to a processor teaching of the flash memory with a decompression circuit of Harari in the flash memory device with a decompression circuit of Dye, in order to provide a removable PC card that can accommodate components offloaded from the host system in order to minimize the size and cost of the host system and to provide flexibility in system configuration (Harari, col. 3, lines 31 – 35).

Dye and Harari disclose all of the limitation discussed above. While they do not specifically disclose that the memory is of synchronous type, synchronous memories and their speed advantage over regular memories were well known at the time of invention. Fallon provides specific evidence of this (Fallon, page 5, paragraph 49).

It would have been obvious to one of ordinary skill in the art, having the teachings of Dye, Harari and Fallon before him at the time the invention was made, to use various forms of high speed memory including an SDRAM in a computer system with non-volatile memory as taught by Fallon in the computer system with non-volatile memory of Dye and Harari, in order to be able to choose from a wider variety of memories. One skilled in the art would easily recognize the benefit of being able to tailor the system depending on the need. For example, a synchronous DRAM is faster that a regular DRAM but costs more. For an applicant that requires higher speed, one would choose an SDRAM. For an application where the speed is not critical, a regular DRAM would be more cost effective.

9. With respect to claims 2 and 7, the memory device (Harari, figure 7, 41 and 60) initiates the data transfer (the controller 41 initiates the data transfer, note the direction of control).

10. With respect to claim 10, Dye, Harari and Fallon do not specifically disclose that the memory is of RDRAM type. However, this particular type of memory, as opposed to the other types of memory, does not have a disclosed purpose nor is it disclosed to overcome any deficiencies in the prior art. Accordingly, it would have been an obvious matter of design choice to use RDRAM type of synchronous memory in the system of Dye, Harari and Fallon, since applicant has not disclosed that the use of RDRAM is to cure any deficiency in the prior art or is for any stated purpose.

11. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Iverson (US Patent No. 6,332,172).

Baltz discloses method of loading a synchronous dynamic random access memory (SDRAM) comprising:

using the SDRAM, initiating a data transfer from a non-volatile memory to the SDRAM memory over a dedicated bus without intervention by another device (see figure 8, transfer is over bus 73 without any other intervening device); and providing a system reset signal from the synchronous memory to a processor after the data has been transferred (col. 7, lines 46 – 60).

However, Baltz does not specifically disclose a flash memory and that the method comprises decompressing of data stored in the flash memory while transferring the data to the synchronous memory. On the other hand, Iverson discloses a method of loading a boot image from a flash memory that decompresses data stored in the non-volatile memory while transferring the data to a memory.

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Iverson before him at the time the invention was made, to use the boot load teachings of the computer system that boots from a non-volatile memory of Iverson in the computer system that boots from a non-volatile memory of Baltz, in order to reduce the system cost (Iverson, col. 2, lines 26 – 31). A compressed RAM image takes up less storage space.

12. Claims 16 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz in view of Iverson and further in view of Harari.

Baltz discloses a processor system power-up method comprising:

detecting a power-up condition with a reset controller and providing a reset signal (figure 4A, 76, see also figure 8, RESET, DC11 – DC13) to an SDRAM memory (col. 6, lines 7 – 9, figure 8, 23 and 100);

using the SDRAM, initiating a data transfer, over a dedicated bus (figure 8, 73) without intervention by another device (figure 8), from a non-volatile memory to the SDRAM memory in

response to the reset signal; and providing a system reset signal from the synchronous memory to a processor after the data has been transferred (col. 7, lines 46 – 60).

However, Baltz does not specifically disclose a flash memory and that the method comprises decompressing of data stored in the flash memory while transferring the data to the synchronous memory. On the other hand, Iverson discloses a method of loading a boot image from a flash memory that decompresses data stored in the non-volatile memory while transferring the data to a memory.

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz and Iverson before him at the time the invention was made, to use the boot load teachings of the computer system that boots from a non-volatile memory of Iverson in the computer system that boots from a non-volatile memory of Baltz, in order to reduce the system cost (Iverson, col. 2, lines 26 – 31). A compressed RAM image takes up less storage space.

Baltz and Iverson disclose all of the limitations discussed above. The only difference between Baltz and Iverson and the claims is that the combination discloses a flash memory and a decompression capability separately while applicant claims an integrated package, i.e. decompression capability and a flash memory in a single package. This is an obvious minor structural variation and making components integral or separable is deem unpatentable (see MPEP 2144.04, IV.B). In addition, Harari specifically discloses a flash memory that

incorporates a decompression capability (figure 5B, 42, col. 8, lines 56 – 62, see also col. 8, line 63 – col. 9, line 7).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz, Iverson and Harari before him at the time the invention was made, to use the removable memory card that incorporate decompression capability in the flash memory of Harari in the computer system with a flash memory and a decompression capability of Baltz and Iverson, in order to provide a removable PC card that can accommodate components offloaded from the host system in order to minimize the size and cost of the host system and to provide flexibility in system configuration (Harari, col. 3, lines 31 – 35).

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dye, Harari and Fallon, and further in view of Baltz.

Dye, Harari and Fallon disclose all of the limitation of the parent claim as discussed above. However, they do not specifically disclose that a system reset signal is provided to the processor after the data is transferred from the flash memory. On the other hand Baltz disclose a processing system where a system reset signal is provided to the processor after the data is transferred from a non-volatile memory (col. 7, lines 46 – 60).

It would have been obvious to one of ordinary skill in the art, having the teachings of Dye, Harari, Fallon, and Baltz before him at the time the invention was made, to use the reset

signal after boot loading from a non-volatile memory teachings of Baltz in the computer system of Dye, Harari and Fallon, in order to overcome the problem of allocating space on a microprocessor for non-volatile memory which is used only during a boot operation (Baltz, col. 1, lines 46 – 48).

14. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Baltz, Iverson, and Harari as applied to claim 16 above and further in view of Shin (US Patent No. 6,735,669).

Claim 16 anticipates all of the limitations of claim 20 with the exception of the type of memory. Balz, Iverson, and Harari disclose all of the limitations of claim 16 as discussed above. However, they do not specifically disclose the use of RDRAM. On the other hand Shin discloses that RDRAM has various operational modes for low power system operation (Shin, col. 1, lines 16 – 20).

It would have been obvious to one of ordinary skill in the art, having the teachings of Baltz, Iverson, Harari and Shin before him at the time the invention was made, to use the lower power consumption RDRAM teachings of Shin in the computer system of Baltz, Iverson and Harari, in order to reduce the overall system power consumption (Shin, col. 1, lines 16 – 20). Reduce power consumption is especially important in battery operated portable computer systems.

Double Patenting

15. In view of the terminal disclaimer filed on January 5, 2005, all double patenting rejections are withdrawn.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
March 2, 2005